# Four and Eight Quadrature Inputs
# M.2 and Mini PCI Express Card
# Hardware Manual

**Models** **M.2-QUAD-8, M.2-QUAD-4, mPCIe-QUAD-8 and mPCIe-QUAD-4**

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MADE IN THE USA

# Chapter 1: Quick Start

It is recommended that you install the software package before installing the card in your computer. You can install the software[1] using either a stand-alone installer downloaded from the website or an optional Software Master CD.

Run the installer you downloaded (or autorun.exe on the Software Master CD) and follow the prompts to install the software for your device.

*Please note: during the installation you may be prompted regarding the installation of non-WHQL-certified drivers; please carefully confirm the digitally signed source of the drivers and accept the installation.*

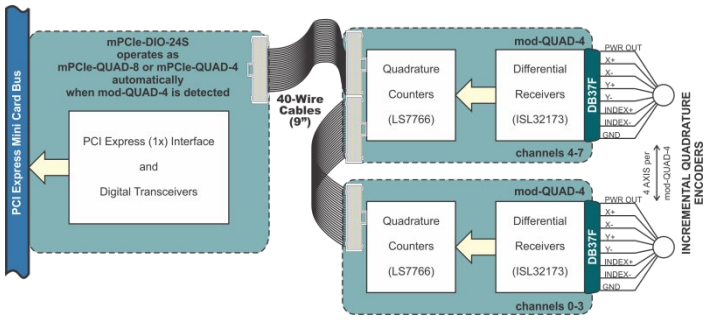
Once the software has been installed, shut down your system and carefully install the mPCIe card. The optional mounting hardware kit accessories include nylon metric screws to secure the non-bus end of the mPCIe card to the mother board. Connect the QUAD module(s) to the mPCIe-DIO board via the provided cable(s).

*Note* The board ships with 3.3V PWR OUT selected. If your encoders require 5V power please consult Chapter 4: Configuration Settings for important information regarding power connections.

Re-start your system. Once the computer finishes booting your new device should already be installed and ready for use; you can confirm this by launching Device Manager and looking under the "Data Acquisition" section. If, for any reason, the mPCIe displays a warning icon, right-click and select "Update Driver".

[1] *In Linux or OSX please refer to github.com/accesio/apci.*

# Chapter 2: Introduction




M.2 and PCI Express Mini Card are low-profile, small-footprint busses standard originally intended for adding peripherals to notebook computers. They have become the de-facto standards for high-performance, small form-factor devices in many applications.

These devices consist of an M.2 or mPCIe interface board that connects to one or two Pico-I/O sized, panel-mountable, DB-37F Quadrature Input Module(s) via included 9" cable(s).

## FEATURES

- Latching I/O connectors
- Accepts 8 or 4 quadrature inputs (A, B & Index (Z))
- Single-ended or differential encoder inputs
- 32-bit counters; count modes include quadrature (x1, x2, x4), free-run, non-quadrature (up/down), non-recycle, modulo-n, and range limit
- Selectable clock source (10Mhz, 20Mhz & 40Mhz) (for digital filtering on inputs)
- Interrupt generation from various status changes
  - select flags for interrupt source (Inst. or Latched)
- 9" cable connects between Quad Module(s) & mPCIe card
- One or two DB-37F Quadrature Input Module(s)

# Chapter 3: Hardware

| This manual applies to the following models: | |
|---|---|
| **M.2 or mPCIe-QUAD-8** | Two 4 Channel Quadrature Input Modules |
| **M.2 or mPCIe-QUAD-4** | 4 Channel Quadrature Input Module |

The M.2 models are M.2 B- & M-key cards in the 2280 size (22 × 80 mm) with a break-away for 2260 (22 × 60 mm). The mPCIe models are full-length "F1" mPCIe devices (30 × 50.95 mm). All units are RoHS compliant.

## INCLUDED IN YOUR PACKAGE

Panel-mount DB-37F Quad Input Module(s) w/screw locks
9" 40-pin cable(s) (228mm)
M.2 or mPCIe Digital I/O card

| Available accessories include: | |
|---|---|
| **ADAP37M** | 37-pin Screw Term board (direct plug-in) |
| **STB-37** | Terminal Board (needs M-F ribbon cable) |
| **mPCIe-HDW-KIT2** | Mounting hardware for 2mm |
| **mPCIe-HDW-KIT2.5** | Mounting hardware for 2.5mm |
| **M.2-HDW-KIT2** | Mounting hardware for 2mm |
| **104e-mPCIe-4A** | PCIe/104 Carrier Board |

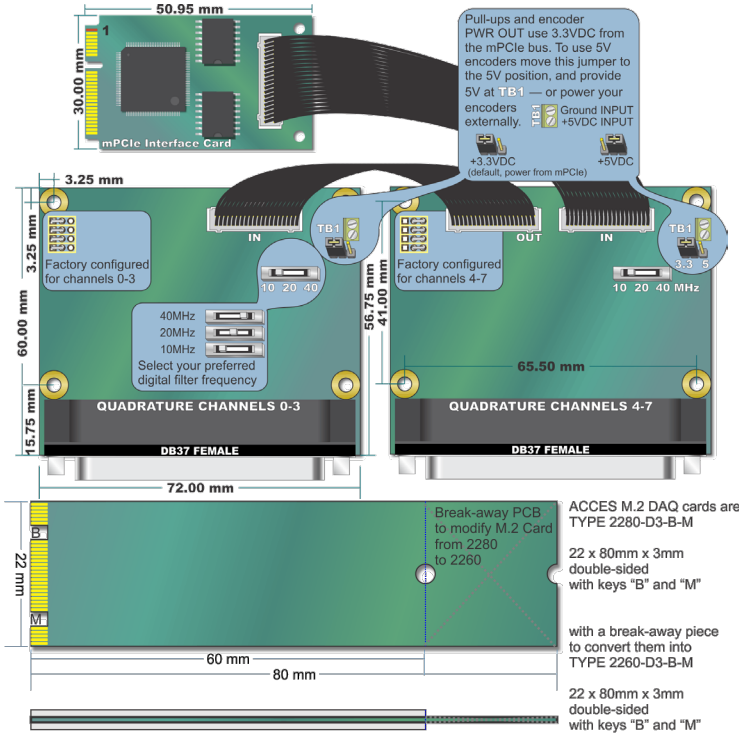
Contact the factory for information regarding additional accessories, options, and specials that may be available to best fit your specific application requirements.

| Available factory options include: | |
|---|---|
| **-T** | Extended Operating Temperature -40 to +85˚C |
| **-CC** | Conformal Coating on board assemblies |

# Chapter 4: Configuration Settings

The QUAD modules need the following configurations:

- Power Select jumpers (see A Note Regarding Encoder Power, below)
- Base Frequency slide switch (40MHz, 20MHz, or 10MHz)




## A NOTE REGARDING ENCODER POWER

Because the bus does not provide +5V the card ships configured to operate at 3.3V, for both on-card circuitry and for use by encoders via the PWR OUT pins on the DB37F connectors (max 300mA total PWR OUT available in this 3.3V-self-powered mode).

The quadrature module is 5V tolerant so if the 5V encoders are *externally* powered (i.e., not powered from PWR OUT pins) no configuration change is necessary, and a mix of 3V and 5V encoders can be connected, with 3V encoders powered from PWR OUT or externally as preferred.

However, you can move the jumper to the 5V position and supply +5V to TB1, which will power the quad module(s) and route +5V from TB1 to the PWR OUT pins.

Note: Each quadrature module (for channels 0-3 or 4-7) requires power to be supplied at TB1; TB1-applied power is not shared between the 4-channel modules. It is thus acceptable to use the 4-channel modules in any combination of 3V/5V modes, as long as the limitations mentioned here are followed.

## CAUTION

**DO NOT connect anything to TB1 while the jumper remains in the 3.3V position, you would be shorting mPCIe bus power to your signal.**

# Chapter 5: PC Interface

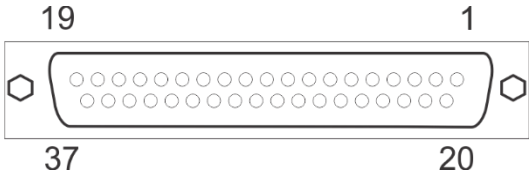
This product interfaces with a PC using either a PCI Express M.2 or PCI Express Mini Card (mPCIe) connection; a small-form-factor, high-performance, rugged peripheral interconnect technology first introduced for use in laptops and other portable computers.

The small size and powerful PCI Express performance, combined with perfect software compatibility with PCIe peripheral designs, has led to their recent adoption as go-to standards for embedded Data Acquisition and Control, and many other applications.

Although M.2 is a broadly adopted industry standard, the actual connection to the computer shares a specification with mSATA: both mSATA and M.2 use the same edge-connector. In fact, well-designed PCs can automatically detect and configure their onboard connectors to work with either M.2 or mSATA devices – and, according to the standards for M.2 and mSATA they are *supposed* to do so! However, some PC manufacturers ship computers that *only* support mSATA devices. Please confirm in your PC documentation that your edge-connector is *actually* PCI Express M.2 Card compliant before installing this, or any, M.2 card.

M.2 and mPCIe define mounting holes for securing the otherwise loose end of the card, so it is impossible for these cards to wiggle or flap themselves loose devices. Eliminating this concern for M.2 and mPCIe cards is a major reason these standards have seen rapid adoption by the Data Acquisition and Control industry.

# Chapter 6: I/O Interface




| DB-37 Female Pinout | | | |
|---|---|---|---|
| 1 | INLO_A0/4 | 20 | INHI_A0/4 |
| 2 | PWR OUT | 21 | INHI_B0/4 |
| 3 | INLO_B0/4 | 22 | GND |
| 4 | PWR OUT | 23 | INHI_Z0/4 |
| 5 | INLO_Z0/4 | 24 | INLO_Z2/6 |
| 6 | NC | 25 | INHI_A2/6 |
| 7 | INLO_A2/6 | 26 | INHI_B2/6 |
| 8 | PWR OUT | 27 | GND |
| 9 | INLO_B2/6 | 28 | INHI_Z2/6 |
| 10 | PWR OUT | 29 | INLO_Z3/7 |
| 11 | INLO_A3/7 | 30 | INHI_A3/7 |
| 12 | PWR OUT | 31 | INHI_B3/7 |
| 13 | INLO_B3/7 | 32 | GND |
| 14 | PWR OUT | 33 | INHI_Z3/7 |
| 15 | INLO_A1/5 | 34 | INHI_A1/5 |
| 16 | PWR OUT | 35 | INHI_B1/5 |
| 17 | INLO_B1/5 | 36 | GND |
| 18 | PWR OUT | 37 | INHI_Z1/5 |
| 19 | INLO_Z1/5 | | |

| Signal | Meanings |
|---|---|
| INLO_Ax | Low side differential "A" input |
| INHI_Ax | High side differential "A" input |
| INLO_Bx | Low side differential "B" input |
| INHI_Bx | High side differential "B" input |
| INLO_Zx | Low side differential "Z" input (Index) |
| INHI_Zx | High side differential "Z" input (index) |
| PWR OUT | Encoder Power Output |
| GND | Ground |

Custom hardware interfaces can be produced to fit your specific application requirement.

| I/O Registers at BAR [2] For Counter 0 | | |
|---|---|---|
| Register offset (decimal) | Write Operation | Read Operation |
| MCR0 [ + 0 ] | Count/Index Function | Count/Index Status |
| MCR1 [ + 1 ] | FLGa/FLGb Function | FLGa/FLGb Status |
| IDR0/ODR0 [ + 2 ] | Input Register 0 | Output Register 0 |
| IDR1/ODR1 [ + 3 ] | Input Register 1 | Output Register 1 |
| IDR2/ODR2 [ +4 ] | Input Register 2 | Output Register 2 |
| IDR3/ODR3 [ +5 ] | Input Register 3 | Output Register 3 |
| STR/TCR [ +6 ] | Load/Set Function | Count Status |
| AXIS Interrupt [ +7 ] | Enable Interrupt | Interrupt Status |
| I/O Registers at BAR [2] For Counter 1 | | |
| Register offset (decimal) | Write Operation | Read Operation |
| MCR0 [ + 8 ] | Count/Index Function | Count/Index Status |
| MCR1 [ + 9 ] | FLGa/FLGb Function | FLGa/FLGb Status |
| IDR0/ODR0 [ + A ] | Input Register 0 | Output Register 0 |
| IDR1/ODR1 [ + B ] | Input Register 1 | Output Register 1 |
| IDR2/ODR2 [ +C ] | Input Register 2 | Output Register 2 |
| IDR3/ODR3 [ +D ] | Input Register 3 | Output Register 3 |
| STR/TCR [ +E ] | Load/Set Function | Count Status |
| AXIS Interrupt [ +F ] | Enable Interrupt | Interrupt Status |

Register tables repeat for Incrementing Axis'.

The following section is an excerpt from the LS7766 datasheet from Oct 2007:

**MCR0**: The MCR0 is an 8-bit read/write register which configures the counting modes and the index input functionality. Upon power-up, the MCR0 is cleared to zero.

| MCR0: | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|---|---|---|---|---|---|---|

B1B0 = 00: Non-quad count mode (A = clock, B = direction)
= 01: x1 quad count mode (one count per quad cycle)
= 10: x2 quad count mode (two counts per quad cycle)
= 11: x4 quad count mode (four counts per quad cycle)

B3B2 = 00: **Free-running** count mode
= 01: **Single-cycle** count mode (CNTR disabled with **carry** and **borrow**, re-enabled with **reset** or **load**)
= 10: **Range-limit** count mode (up and down count ranges are limited between IDR and zero, respectively. Counting freezes at these limits but resumes when the direction is reversed)
= 11: **Modulo-n** count mode (input count clock frequency is divided by a factor of [n+1], where n = IDR. In up direction, the CNTR is **cleared** to 0 at CNTR = IDR and up count continues. In down direction, the CNTR is preset to the value of IDR at CNTR = 0 and down count continues. A mod-n rollover marker pulse is generated at each limit at the FLGa output).

B5B4 = 00: Disable INDX/ input
= 01: Configure INDX/ input as the load_CNTR input (transfers IDR to CNTR)
= 10: Configure INDX/ as the reset _CNTR input (clears CNTR to 0)
= 11: Configure INDX/ as the load_ODR input (transfers CNTR to ODR)

B6 = 0: Asynch index
= 1: Synch. index (overridden in non-quad mode)

B7 = 0: Input filter clock (PCK) division factor = 1. Filter clock frequency = fPCK
= 1: Input filter clock division factor = 2. Filter clock frequency = fPCK/2.

**MCR1**: The MCR1 is an 8-bit read/write register which configures the FLGa and FLGb output functionality. In addition, the MCR1 can be used to enable/disable counting. Upon power-up, the MCR1 is cleared to zero:.

| MCR1: | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|---|---|---|---|---|---|---|

B0 = 1: Enable Carry on FLGa (flags CNTR overflow; latched or unlatched logic low on carry)

B1 = 1: Enable Borrow on FLGa (flags CNTR underflow, latched or unlatched logic low on borrow)

B2 = 1: Enable Compare on FLGa (In free-running count mode a latched or unlatched logic low is generated in both up and down count directions at CNTR = IDR. In contrast, in range-limit and mod-n count modes a latched or unlatched low is generated at CNTR = IDR in the up-count direction only.

B3 = 1: Enable index on FLGa (flags index, latched or unlatched logic low when INDX input is active)

B5B4 = 00: FLGb disabled (fixed high)
= 01: FLGb = **Sign**, high for negative signifying CNTR underflow, low for positive.
= 10: FLGb = Up/Down count direction, high in count-up, low in count-down

B6 = 0: Enable counting
= 1: Disable counting

B7 = 0: FLGa is latched
= 1: FLGa is non-latched and instantaneous

**NOTE:** Carry, Borrow, Compare and Index can all be simultaneously enabled on FLGa.

**IDR**

The IDR is a 32-bit data register directly addressable for write. In the octal bus-configuration, the input data is written in byte segments of byte0 (IDR0), byte1 (IDR1), byte2 (IDR2) and byte3 (IDR3). In the hex bus-configuration the data is written in word segments of word0 (IDR1:IDR0) and word1 (IDR3:IDR20).

B31----------B0

| IDR: | IDR3 | IDR2 | IDR1 | IDR0 |
|---|---|---|---|---|
| | B7----B0 | B7----B0 | B7----B0 | B7----B0 |
| | --byte3-- | --byte2-- | --byte1-- | --byte0-- |
| | --------word1------- | | --------word0------- | |

The IDR serves as the input portal for the counter (CNTR) since the CNTR is not directly addressable for either read or write. In order to preset the CNTR to any desired value the data is first written into the IDR and then transferred to the CNTR. In **mod-n** and **range-limit** count modes the IDR serves as the repository for the division factor n and the count range-limit, respectively. The IDR can also be used to hold a target position data for comparing with the running CNTR.

A compare equality flag is generated at IDR = CNTR to signal the event of arriving at the target.

**CNTR:**

The CNTR is a 32-bit up/down counter which counts the up/down pulses resulting from the quadrature clocks applied at A and B inputs or alternatively, in nonquadrature mode, pulses applied at the A input. The CNTR is not directly accessible for read or write; instead it can be preloaded with data from the IDR or it can port its own data out to the ODR which in turn can be accessed by read operation. In both quadrature and nonquadrature modes, the CNTR can be further configured into either free-running or single-cycle or mod-n or range-limit mode. In quadrature mode, the count resolution is programmable to be x1 or x2 or x4 of the A quad B cycles.

**ODR:**

The ODR is a 32-bit data register directly addressable for read. In the octal bus-configuration, the output data is read in byte segments of byte0 (ODR0), byte1 (ODR1), byte2 (ODR2), and byte3 (ODR3). In the hex bus configuration the data is read in word segments of word0 (ODR1:ODR0) and word1 (ODR3:ODR2).

B31----------B0

| ODR: | ODR3 | ODR2 | ODR1 | ODR0 |
|---|---|---|---|---|
| | B7----B0 | B7----B0 | B7----B0 | B7----B0 |
| | --byte3-- | --byte2-- | --byte1-- | --byte0-- |
| | --------word1------- | | --------word0------- | |

**STR**

The STR is an 8-bit status register indicating count related status.

| +E | Dir | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|---|---|---|---|---|---|---|---|
| STR: | RW | CY | BW | CMP | IDX | CEN | 0 | U/D | S |

An individual STR bit is set to 1 when the bit related event has taken place. The STR is cleared to 0 at power-up. The STR can also be cleared through the control register TCR with the exception of bit_1(U/D) and bit3_(CEN). These two STR bits always indicate the instantaneous status of the count_direction and count_enable assertion/de-assertion.

The STR bits are described below:

- B7 (CY): Carry; set by CNTR overflow
- B6 (BW): Borrow; set by CNTR underflow
- B5 (CMP): Set when CNTR = PR
- B4 (IDX): Set when INDX input is at active level
- B3 (CEN): Set when counting is enabled, reset when disabled
- B2 (0): Always 0
- B1 (U/D): Set when counting up, reset when counting down
- B0 (S): Sign of count value; set = negative, reset = positive

**TCR:**

The TCR is a write only register, which when written into, generates transient signals to perform load and reset operations as described below:

TCR: B7 B6 B5 B4 B3 B2 B1 B0

- B0 = 0: Nop
  = 1: Reset CNTR to 0.
  (Should not be combined with load_CNTR operation)
- B1 = 0: Nop
  = 1: Load CNTR from IDR. Affects all 32 bits.
  (Should not be combined with reset_CNTR operation)
- B2 = 0: Nop
  = 1: Load ODR from CNTR. Affects all 32 bits
- B3 = 0: Nop
  = 1: Reset STR.
  Affects status bits for carry, borrow, compare and index. Status bits corresponding to count_enable, count direction and sign are not affected.
- B4 = 0: Nop.
  = 1: Master reset. Resets MCR0, MCR1, IDR, ODR, STR
- B5 = 0: Nop
  = 1: Set sign bit (STR bit0)
- B6 = 0: Nop
  = 1: Reset sign bit (STR bit0)
- B7 = x: Not used.

**FCR:**

The FCR is a read/write register, which enables interrupts. When read, it returns global and local interrupt status and indicates instantaneous local interrupt count.

FCR: B7 B6 B5 B4 B3 B2 B1 B0

- B0 = 0: Always 0 (not used)
- B1 = 0: Interrupts disabled
  = 1: Interrupts enabled
- B2 = 0: Always 0 (not used)
- B3 = 0: No local (LS7766) interrupt*
  = 1: Local (LS7766) interrupt generated*
- B4 LSB Instantaneous Interrupt count
- B5 Instantaneous interrupt count
- B6 MSB Instantaneous interrupt count
- B7 = 0: No Global interrupt
  = 1: Global interrupt generated

***FLGa and FLGb on Counter 0 and Counter 1 (BASE +0 to BASE +F) are all "ANDed" together. If only counter 0 interrupt is enabled, and a flag is generated on that counter, that corresponding interrupt status will become active on counter 1. This is also true if counter 1 was enabled and counter 0 is disabled. This is the same for counter 2 and counter 3 (+17 to +1F), counters 4 and 5 (+27 to +2F), and for counter 6 and 7 (+37 to +3F).**

*In addition to the I/O registers at BAR[2], BAR[0] also contains two registers.*

*One register for compatibility with the PCIe product line: Register +0x69 contains a read-only status bit [d7] which indicates the card is generating an IRQ when set [1], and is not generating an IRQ when clear [0].*

All of these registers can be operated from any operating system using any programming language, using either no driver at all (kernel mode, Linux ioperm(3), DOS, etc.) or using one of the ACCES provided drivers (AIOWDM [for Windows], APCI [for Linux & OSX]), or using any 3rd party APIs such as provided with Real-Time OSes.

In Windows[1], please consult the various samples (C#, Delphi, VC6, VB6, and more) to explore how to program the device. The Software Reference Manual.pdf provides reference material covering all AIOWDM driver APIs, and tips for simplifying tasks such as Plug-and-Play card detection. Please note that the Software Reference Manual.pdf will include numerous functions that don't apply to this device. A quick reference of the most-applicable functions is provided, below:

| AIOWDM API Quick Reference | |
|---|---|
| **Function name** | **Function Purpose** |
| `RelInPortB()` | Read 8-bits of data |
| `RelOutPortB()` | Write 8-bits of data |
| `GetNumCards()` | Determine how many cards AIOWDM has detected in the system |
| `WaitForIRQ()` | Block the thread until the device reports a change-of-state has occurred on a pin of an enabled I/O group (or the wait is aborted). |

There are quite a few additional functions provided by AIOWDM.dll; please consult the Software Reference manual (.pdf), and/or the sample programs, for more information.

Under certain circumstances the following might prove useful:

| PCI Express Mini Card Plug-and-Play Data | |
|---|---|
| **Vendor / Device ID** | **Card Type** |
| **0x494F / 0x010A** | M.2 or mPCIe QUAD-4 |
| **0x494F / 0x010B** | M.2 or mPCIe QUAD-8 |

## Available Downloads

The latest information can always be found on the product page on the website. Here are some useful links:

| Links to useful downloads | |
|---|---|
| **Main site** | https://accesio.com |
| **Product's page** | accesio.com/mPCIe-QUAD-8<br>accesio.com/M.2-QUAD-8 |
| **This manual** | accesio.com/MANUALS/M.2-_mPCIe-QUAD-8.pdf |
| **Windows Software Install Package** | accesio.com/files/packages/M.2-_mPCIe-QUAD-8 Install.exe |

[1] *In Linux or OSX please refer to the documentation at* github.com/accesio/APCI.

# CHAPTER 8: SPECIFICATIONS

## PC Interface

| | |
|---|---|
| PCI Express Mini Card | Type F1 "Full Length" V1.2 |
| M.2 PCI Express | 2280/2260 B+M-key |

Note: Device's connector violates component height restrictions

## Input Section

| | |
|---|---|
| Counters | 8 (or 4) |
| Receiver Type | ISL32173 |
| Configuration | Phase A, B and Index; differential or S.E. inputs |
| Common mode | -7V to 12V |
| Hysteresis | 30mV typical |
| Sensitivity | +/-200mV |
| Impedance | Internal 48kΩ minimum |
| Bias | Non-inverting 4.7kΩ to Vcc<br>Inverting 2.35kΩ to Gnd |
| Compatibility | 5V logic tolerant at 3.3VDC |

## Counter Section

| Type | LS7766 32-bit Dual Axis Quadrature Counter | |
|---|---|---|
| | **5VDC Input** | **3.3VDC Input** |
| Quad (A&B) inputs | 9.6MHz maximum | 4.5MHz maximum |
| Separation | 26ns minimum | 52ns minimum |
| A&B pulse width | 52ns minimum | 105ns minimum |
| Index pulse width | 32ns minimum | 60ns minimum |
| | | |
| Non-Quad (A) input | 40MHz maximum | 20MHz maximum |
| Low/Hi pulse width | 12ns minimum | 24ns minimum |
| B input (direction) | 12ns min setup time<br>10ns min hold time | 24ns min setup time<br>20ns min hold time |
| Index pulse width | 32ns minimum | 30ns minimum |
| | | |
| Slide Switch 40MHz | MCR0 Bit 7 Low = 40MHz | MCR0 Bit 7 High = 20MHz |
| Slide Switch 20MHz | MCR0 Bit 7 Low = 20MHz | MCR0 Bit 7 High = 10MHz |
| Slide Switch 10MHz | MCR0 Bit 7 Low = 10MHz | MCR0 Bit 7 High = 5MHz |

## FPGA Controller Register (FCR)

Interrupt Source: LS7766 FLGa/FLGb Outputs

FLGa Sources: Index, Carry, Borrow, Compare

FLGb Sources: Sign, Up/Down Counter

I/O Address Space: 8 bytes per counter, 64 bytes for 8 counter-board

## Environmental

| | | |
|---|---|---|
| Temperature | Operating | 0°C to 70°C (order "-T" for -40° to 85°C) |
| | Storage | -65° to 150°C |
| Humidity | | 5% to 95%, non-condensing |
| Power required<br>*note: max current specs do not include encoder power | mPCIe card | +3.3VDC @360mA (typ)<br>+3.3VDC @430mA when powering one Quad Module from mPCIe bus power<br>+3.3VDC @500mA when powering two Quad Modules from mPCIe bus power |
| | 3.3V bus power to encoders | 300mA max |
| | Quad Mod | +5.0VDC @165mA (typ) plus encoder current<br>+5.0VDC @290mA (max) plus encoder current |

## Physical

| Board characteristics | | |
|---|---|---|
| Weight | | 6.2 grams (mPCIe) 5.4 grams (M.2) |
| Size, mPCIe | Length | 50.95 mm (2.006") |
| | Width | 30.00 mm (1.181") |
| Size, M.2 | Length | 80 mm or 60 mm |
| | Width | 22 mm |
| I/O connector | On-card mating | Molex 501190-4017 40-pin latching<br>Molex 501189-4010 |
| **QUAD Module characteristics** | | |
| Weight | | 44.8 grams (+11.2g for the 9" cable) |
| Size | Length | 2.835" |
| | Width | 2.362" |
| I/O connector | On-module mating | Female, D-Sub Miniature, 37-pin<br>Male, D-Sub Miniature, 37-pin |
| Interface connector | On-card mating | Molex 501190-4017 40-pin latching<br>Molex 501189-4010 |

# CHAPTER 9: CERTIFICATIONS

### CE & FCC

These devices are designed to meet all applicable EM interference and emission standards. However, as they are intended for use installed on motherboards, and inside the chassis of industrial PCs, important care in the selection of PC and chassis is important to achieve compliance for the computer as a whole.

### UL & TUV

No AC or DC voltages above 31V are consumed or produced during normal operation of this device. This product is therefore exempt from any related safety standards. Use it with confidence!

### ROHS / LEAD-FREE STATEMENT

All models are produced in compliance with RoHS and various other lead-free initiatives.

## WARNING

**A SINGLE STATIC DISCHARGE CAN DAMAGE YOUR CARD AND CAUSE PREMATURE FAILURE! PLEASE FOLLOW ALL REASONABLE PRECAUTIONS TO PREVENT A STATIC DISCHARGE SUCH AS GROUNDING YOURSELF BY TOUCHING ANY GROUNDED SURFACE PRIOR TO TOUCHING THE CARD.**

**ALWAYS CONNECT AND DISCONNECT YOUR FIELD CABLING WITH THE COMPUTER POWER OFF. ALWAYS TURN COMPUTER POWER OFF BEFORE INSTALLING A CARD. CONNECTING AND DISCONNECTING CABLES, OR INSTALLING CARDS, INTO A SYSTEM WITH THE COMPUTER OR FIELD POWER ON MAY CAUSE DAMAGE TO THE I/O CARD AND WILL VOID ALL WARRANTIES, IMPLIED OR EXPRESSED.**

## WARRANTY

Prior to shipment, ACCES equipment is thoroughly inspected and tested to applicable specifications. However, should equipment failure occur, ACCES assures its customers that prompt service and support will be available. All equipment originally manufactured by ACCES which is found to be defective will be repaired or replaced subject to the following considerations:

### GENERAL

Under this Warranty, liability of ACCES is limited to replacing, repairing or issuing credit (at ACCES discretion) for any products which are proved to be defective during the warranty period. In no case is ACCES liable for consequential or special damage arriving from use or misuse of our product. The customer is responsible for all charges caused by modifications or additions to ACCES equipment not approved in writing by ACCES or, if in ACCES opinion the equipment has been subjected to abnormal use. "Abnormal use" for purposes of this warranty is defined as any use to which the equipment is exposed other than that use specified or intended as evidenced by purchase or sales representation. Other than the above, no other warranty, expressed or implied, shall apply to any and all such equipment furnished or sold by ACCES.

### TERMS AND CONDITIONS

If a unit is suspected of failure, contact ACCES' Customer Service department. Be prepared to give the unit model number, serial number, and a description of the failure symptom(s). We may suggest some simple tests to confirm the failure. We will assign a Return Material Authorization (RMA) number which must appear on the outer label of the return package. All units/components should be properly packed for handling and returned with freight prepaid to the ACCES designated Service Center, and will be returned to the customer's/user's site freight prepaid and invoiced.

### COVERAGE

*FIRST THREE YEARS:* Returned unit/part will be repaired and/or replaced at ACCES option with no charge for labor or parts not excluded by warranty. Warranty commences with equipment shipment.

*FOLLOWING YEARS*: Throughout your equipment's lifetime, ACCES stands ready to provide on-site or in-plant service at reasonable rates similar to those of other manufacturers in the industry.

### EQUIPMENT NOT MANUFACTURED BY ACCES

Equipment provided but not manufactured by ACCES is warranted and will be repaired according to the terms and conditions of the respective equipment manufacturer's warranty.

## DISCLAIMER

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